Study of a Class of Sampled-Data ILC from the Point of Performance Improvement and Memory Capacity

Chiang-Ju Chien and Ya-Syuan Shu

Abstract— **This paper presents the design and application of a sampled-data iterative learning control combing feedback and feedforward learning mechanism for nonlinear systems with initial resetting error, input disturbance and output measurement noise. Firstly, a new technical result is rigorously studied to show that the tracking error will converge to a residual set if a sufficient condition is satisfied and the sampling period is small enough. The sufficient condition is guaranteed by a forgetting factor and the feedforward learning gain. Secondly, three types of sampled-data iterative learning controllers are considered from both performance improvement and memory capacity point of view based on the derived technical results. In order to demonstrate the correctness and feasibility, the proposed sampled-data iterative learning controllers are realized by a digital circuit in an FPGA chip and applied to a repetitive position tracking control of DC motor. The experimental results show the effectiveness of the three types sampled-data iterative learning controllers. Comparisons of learning performance and memory capacity are also studied extensively.**

I. INTRODUCTION

Iterative learning control (ILC) [1-2] has been known to be one of the most effective control strategies for control systems to execute repeated tracking control tasks. To begin with, the basic PID-type iterative learning controllers [3-6] were developed. The learning control input is updated by a learning law constructed by the information of error and input in the previous iteration. The control performance over the entire control time interval by the PID-type ILC is improved without using accurate system model. Many implementations have also been developed [7-12] for industrial applications.

Among the existing PID-type ILCs, the discrete-time ILCs [13-16] attract a lot of attentions. The main reason is that ILC system has to store a lot of data in the memory for input adaptation so that it is more practical to design and analyze the iterative learning system in discrete-time domain. For discrete -time ILC, the control plant is actually modeled as a discrete-time system. As most of the control plants are continuous-time systems, the sampled-data ILC, i.e., the plant is modeled as a continuous-time system and the controller is designed as a discrete-time algorithm, has been studied in [17-19]. In sampled-data ILCs, the sampler and zero order holder are usually utilized for the transformation between continuous-time signals and discrete-time signals.

In addition to the studies of different implementation approaches of ILCs, the robustness issues, performance improvement of learning error, or even the reduce of memory capacity for storage were widely discussed in the literatures. For the issue of performance improvement, it is well known that the learning error of traditional feedforward ILCs is likely to grow quite significantly before it converges to zero in the process of learning and the rate of convergence is often slow. This behavior is mainly due to the fact that the ILC structure is basically an open loop system which does not compensate for the output error in each trial. Hence, one of the possible approaches to solve this problem is to use both the current error and previous error to update the current control input [20-23]. However, the feedforward ILC combining the current error structure can not reduce the memory capacity as addressed in our previous work [24]. In [24], we tried to used only current error information to design the sampled-data ILC such that the size of memory capacity can be greatly reduced.

In this paper, we aim to study the most practical design of sampled-data ILC for application to position tracking of DC motors under the consideration of both performance improvement and memory capacity. A combination of feedback stabilization control and feedforward iterative learning control will be presented. In other words, both current error data and previous error data will be applied in the proposed sampled-data ILC. A new technical result is rigorously shown that the tracking error will converge to a residual set even the system exists initial resetting error, input disturbance and output measurement noise if a sufficient condition is satisfied and the sampling period is small enough. The sufficient condition is guaranteed by a forgetting factor and the feedforward learning gain. Based on the derived technical theory, three types of sampled-data ILCs are discussed and an optimal design for both performance improvement and memory capacity is suggested for real implementation. To prove the correctness and effectiveness of the theoretical results, the proposed three types of sampled-data ILC algorithms are then implemented by a digital circuit with an application to repetitive position tracking control of DC motors. We use VHDL as a design tool to realize the digital circuit. The circuit is then downloaded into an FPGA chip as the controller for the experiment. According to the experimental results, we prove that the

This work is supported by National Science Council, R.O.C., under Grant MOST 104-2221-E-211-010.

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978-1-4673-9714-8/16/$31.00 ©2016 IEEE

theoretical results and the corresponding digital circuit are correct and feasible.

II. CONTROL OBJECTIVE AND ILC DESIGN

In this paper, the following class of nonlinear systems is considered to execute a repetitive control task over a finite time interval $[0,T]$

$$\begin{aligned}\dot{x}_i(t) &= f(x_i(t)) + Bu_i(t) + \omega_i(t) \\ y_i(t) &= Cx_i(t) + \xi_i(t)\end{aligned} \tag{1}$$

In (1), $x_i(t) \in R^{n\times 1}$ is the state, $y_i(t) \in R^{m\times 1}$ is the output, $u_i(t) \in R^{m\times 1}$ is the input, $\omega_i(t) \in R^{n\times 1}$ is a random input disturbance, $\xi_i(t) \in R^{m\times 1}$ is a random output measurement noise, $f(x_i(t)) \in R^{n\times 1}$ is the system nonlinearity, $B \in R^{n\times m}$ is the input gain matrix, and $C \in R^{n\times m}$ is the output gain matrix. The index i denotes the iteration number and $t \in [0,T]$. We define h as the sampling period of the digital control system with the sampling instant $n = 0,1,2,\cdots,N$ and $Nh = T$, where N is a positive integer. A sampler and hold is utilized for the digital control system so that the control input $u_i(t)$ satisfies $u_i(t) = u_i(nh)$ for $nh \le t < (n+1)h$. A realizable desired output $y_d(t) \in R^{m\times 1}$ which satisfies the following equation without input disturbance and output measurement noise is given as

$$\begin{aligned}\dot{x}_d(t) &= f(x_d(t)) + Bu_d(t) \\ y_d(t) &= Cx_d(t)\end{aligned} \tag{2}$$

where $u_d(t)$ is an unknown desired input satisfying $u_d(t) = u_d(nh)$, $nh \le t < (n+1)h$. The control objective is to design a sampled-data iterative learning controller $u_i(nh)$ such that the output error at each sampling instant satisfies

$$\lim_{i\to\infty} \|y_d(nh) - y_i(nh)\| < \sigma \;, \forall n \in \{0,1,2,\cdots,N\}$$

where σ denotes a certain error tolerance bound. To achieve the control objective, the following assumptions are given.

(A1) The coupling matrix CB is nonsingular.

(A2) There exists an unknown constant ℓ_1 such that $\|f(x_1(t)) - f(x_2(t))\| \le \ell_1 \|x_1(t) - x_2(t)\|$.

(A3) The initial state $x_i(0)$, input disturbance $\omega_i(nh)$ and output noise $\xi_i(nh)$ satisfy $\|x_d(0) - x_i(0)\| \le \varepsilon_1$, $\|\omega_i(nh)\| \le \varepsilon_2$, $\|\xi_i(nh)\| \le \varepsilon_3$, for $i = 0,1,2,\cdots,\infty$, $n = 0,1,2,\cdots,N$, and ε_1, ε_2, ε_3 are positive constants.

(A4) The desired output $y_d(nh)$ and desired input $u_d(nh)$ are bounded with $d = \max_{n\in\{0,1,2,\cdots,N\}} \|u_d(nh)\|$.

The sampled-data iterative learning controller $u_i(nh)$ in this work is designed with a feedback stabilization controller $u_i^b(nh)$ and a feedforward iterative learning controller $u_i^f(nh)$ as follows,

$$u_i(nh) = u_i^b(nh) + u_i^f(nh) \tag{3}$$

1. <u>Feedback stabilization controller</u>

$u_i^b(nh)$ is designed as any dynamic or static feedback controller which stabilizes the system (1). It takes the following general form of

$$\begin{aligned}z_i((n+1)h) &= p(z_i(nh)) + q(z_i(nh))e_i(nh) \\ u_i^b(nh) &= r(z_i(nh)) + s(z_i(nh))e_i(nh)\end{aligned} \tag{4}$$

where $z_i(nh) \in R^{n_1}$ is the state vector. The functions $p: R^{n_1} \to R^{n_1}$ and $r: R^{n_1} \to R^{n}$ must satisfy $\|p(z_i(nh))\| \le p_0 \|z_i(nh)\|$ and $\|r(z_i(nh))\| \le r_0 \|z_i(nh)\|$, for some $p_0, r_0 > 0$. Furthermore, the functions $q: R^{n_1} \to R^{n_1\times n}$ and $s: R^{n_1} \to R^{n\times n}$ must satisfy $\|q(z_i(nh))\| \le q_0$, $\|s(z_i(nh))\| \le s_0$, for some $q_0, s_0 > 0$.

2. <u>Feedforward iterative learning controller</u>

$u_i^f(nh)$ is designed as a D-type like ILC ,

$$\begin{aligned}u_i^f(nh) &= (1-\alpha)u_{i-1}(nh) + \alpha u_0(nh) \\ &\quad + L_{i-1}(nh)(e_{i-1}((n+1)h) - e_{i-1}(nh))\end{aligned} \tag{5}$$

where $u_i^f(nh)$ is the feedforward iterative learning input at the sampling time nh of i th iteration, $u_{i-1}(nh)$ is the total input at the sampling time nh of ($i-1$)th iteration, $u_0(nh)$ is the initial input, $0 < \alpha < 1$ is a forgetting factor, $e_{i-1}((n+1)h)$ is the output error at sampling time $(n+1)h$ of ($i-1$)th iteration, in other words, $e_{i-1}((n+1)h) = y_d((n+1)h) - y_{i-1}((n+1)h)$ for $n = 0,1,2,...,N-1$. $L_{i-1}(nh)$ is the learning gain which satisfies

$$\sup_{n\in\{0,1,...,N\}} \sup_{i\in\{1,2,\cdots,\infty\}} \|L_{i-1}(nh)\| \le \ell$$

for some positive constant ℓ.

III. MAIN RESULT OF CONVERGENCE ANALYSIS

Define the state error and input error as $\delta x_i(t) \equiv x_d(t) - x_i(t)$ and $\delta u_i(t) \equiv u_d(t) - u_i(t)$. For $t \in [nh,(n+1)h]$, we have

$$\begin{aligned}& x_d(t) - x_i(t) \\ &= x_d(nh) - x_i(nh) + \int_{nh}^{t} (\dot{x}_d(\tau) - \dot{x}_i(\tau))d\tau \\ &= \delta x_i(nh) + \int_{nh}^{t} (f(x_d(t)) - f(x_i(\tau)) + B\delta u_i(\tau) - \omega_i(\tau))d\tau\end{aligned}$$

Use the assumption (A2), the fact of $\delta u_i(t) = \delta u_i(nh)$, $t \in [nh,(n+1)h)$, and let $\|B\| = b$, then we have

$$\begin{aligned}\|\delta x_i(t)\| &\le \|\delta x_i(nh)\| + \int_{nh}^{t} \left(\ell_1 \|\delta x_i(\tau)\| + b\|\delta u_i(\tau)\| + \varepsilon_2\right) d\tau \\ &\le \|\delta x_i(nh)\| + \ell_1 \int_{nh}^{t} \|\delta x_i(\tau)\| d\tau + bh\|\delta u_i(nh)\| + \varepsilon_2 h\end{aligned} \tag{6}$$

By using Bellman-Gronwall Lemma, (6) can be rewritten as

$$\begin{aligned}\|\delta x_i(t)\| &\le e^{\ell_1 t}\left(\|\delta x_i(nh)\| + bh\|\delta u_i(nh)\| + \varepsilon_2 h\right) \\ &\le a_1\|\delta x_i(nh)\| + a_2 h\|\delta u_i(nh)\| + a_1\varepsilon_2 h\end{aligned} \tag{7}$$

For some positive constants a_1 and a_2. Finally, let the time $t = (n+1)h$, we have

$$\|\delta x_i((n+1)h)\| \le a_1\|\delta x_i(nh)\| + a_2 h\|\delta u_i(nh)\| + a_1\varepsilon_2 h \tag{8}$$

Next, we can find that the output error between two successive sampling instants will satisfy the following equation,

$$\begin{aligned}
&e_{i-1}((n+1)h)\\
&= y_d((n+1)h) - y_{i-1}((n+1)h)\\
&= y_d((n+1)h) - Cx_{i-1}((n+1)h) - \xi_{i-1}((n+1)h)\\
&= y_d(nh) - Cx_{i-1}(nh) + \int_{nh}^{(n+1)h} (C\dot{x}_d(\tau) - C\dot{x}_{i-1}(\tau))d\tau\\
&\quad - \xi_{i-1}((n+1)h)\\
&= y_d(nh) - Cx_{i-1}(nh) - \xi_{i-1}(nh)\\
&\quad + C\int_{nh}^{(n+1)h} (f(x_d(\tau)) - f(x_{i-1}(\tau)) + B(u_d(\tau) - u_{i-1}(\tau))\\
&\quad - \omega_{i-1}(\tau))d\tau - \xi_{i-1}((n+1)h) + \xi_{i-1}(nh)\\
&= e_{i-1}(nh) + C\int_{nh}^{(n+1)h} \left(f(x_d(\tau)) - f(x_{i-1}(\tau)) - \omega_{i-1}(\tau)\right)d\tau\\
&\quad + CBh\delta u_{i-1}(nh) - \xi_{i-1}((n+1)h) + \xi_{i-1}(nh)
\end{aligned} \tag{9}$$

Theorem 1: Let the system (1) satisfy the assumptions (A1), (A2), (A3) and desired input as well as desired output satisfy assumption (A4). If we apply the sampled- data iterative learning controller (3), (4), (5) with the following condition being satisfied

$$\sup_{i\in\{1,2,\cdots,\infty\}} \sup_{n\in\{0,1,\ldots,N\}} \|(1-\alpha)I - L_i(nh)CBh\| \le \overline{\rho} < 1 \tag{10}$$

then we guarantee that

$$\lim_{i\to\infty} \|y_d(nh) - y_i(nh)\| \le \sigma, \forall n \in \{0,1,\cdots,N\}$$

for some positive constant σ depending on $\varepsilon_1, \varepsilon_2, \varepsilon_3$ and α.

Proof: In the following technical analysis, we use n to replace nh in the following derivation for simplicity. The forward input error $u_d(n) - u_i^f(n)$ is derived by using (9) as follows,

$$\begin{aligned}
&u_d(n) - u_i^f(n)\\
&= u_d(n) - (1-\alpha)u_{i-1}(n) - \alpha u_0(n) - L_{i-1}(n)\left(e_{i-1}(n+1) - e_{i-1}(n)\right)\\
&= \left((1-\alpha)I - L_{i-1}(n)CBh\right)(u_d(n) - u_{i-1}(n)) - \alpha u_0(n)\\
&\quad - L_{i-1}(n)C\int_n^{n+1} \left(f(x_d(\tau)) - f(x_{i-1}(\tau)) - \omega_{i-1}(\tau)\right)d\tau\\
&\quad - L_{i-1}(n)\xi_{i-1}(n+1) + L_{i-1}(n)\xi_{i-1}(n)
\end{aligned} \tag{11}$$

Taking norms on (11) and using (7), (10), we have

$$\begin{aligned}
&\|u_d(n) - u_i^f(n)\|\\
&\le \|(1-\alpha)I - L_{i-1}(n)CBh\| \|u_d(n) - u_{i-1}(n)\|\\
&\quad + \ell c \ell_1 \int_n^{n+1} \|\delta x_{i-1}(\tau)\| d\tau + \ell c \varepsilon_2 h + 2\ell\varepsilon_3 + \alpha\|\delta u_0(n)\|\\
&\le (\overline{\rho} + \ell c \ell_1 a_2 h^2)\|\delta u_{i-1}(n)\| + k_1\|\delta x_{i-1}(n)\| + k_2
\end{aligned} \tag{12}$$

where $\rho = \overline{\rho} + \ell c\ell_1 a_2 h^2$, $k_1 = \ell c\ell_1 h a_1$, $k_2 = \ell c\varepsilon_2 h + 2\ell\varepsilon_3 + \alpha \max_n \|\delta u_0(n)\| + \ell c\ell_1 a_1 \varepsilon_2 h^2$. It is noted that we can still ensure $\rho < 1$ if h is chosen to small enough. Now according to (4), the norm of $u_{i-1}^b(n)$ will satisfy

$$\begin{aligned}
\|u_{i-1}^b(n)\| &\le \|r(z_{i-1}(n))\| + \|s(z_{i-1}(n))\| \|e_{i-1}(n)\|\\
&\le r_0\|z_{i-1}(n)\| + s_0 c\|\delta x_{i-1}(n)\| + s_0\varepsilon_3
\end{aligned} \tag{13}$$

Substituting (13) into (12), it yields

$$\begin{aligned}
&\|u_d(n) - u_i^f(n)\|\\
&\le \rho\|u_d(n) - u_{i-1}^f(n)\| + \rho r_0\|z_{i-1}(n)\| + (\rho s_0 c + k_1)\|\delta x_{i-1}(n)\|\\
&\quad + \rho s_0\varepsilon_2 + k_2\\
&\le \rho\|u_d(n) - u_{i-1}^f(n)\| + g\left(\|z_{i-1}(n)\| + \|\delta x_{i-1}(n)\|\right) + k_3
\end{aligned} \tag{14}$$

where $g = \max\{\rho r_0, \rho s_0 c + k_1\}$, $k_3 = \rho s_0\varepsilon_2 + k_2$. Next, we investigate the signal properties of $\|z_{i-1}(n)\|$ and $\|\delta x_{i-1}(n)\|$. According to (4), we have

$$\begin{aligned}
\|z_{i-1}(n)\| &\le p_0\|z_{i-1}(n-1)\| + q_0\|e_{i-1}(n-1)\|\\
&\le p_0\|z_{i-1}(n-1)\| + q_0 c\|\delta x_{i-1}(n-1)\| + q_0\varepsilon_3
\end{aligned} \tag{15}$$

Using (8), we can derive that

$$\begin{aligned}
&\|\delta x_{i-1}(n)\|\\
&\le a_1\|\delta x_{i-1}(n-1)\| + a_2 h\|\delta u_{i-1}(n-1)\| + a_1\varepsilon_2 h\\
&\le a_1\|\delta x_{i-1}(n-1)\| + a_2 h\|u_d(n-1) - u_{i-1}^f(n-1)\|\\
&\quad + a_2 h\left(r_0\|z_{i-1}(n-1)\| + s_0 c\|\delta x_{i-1}(n-1)\| + s_0\varepsilon_3\right) + a_1\varepsilon_2 h
\end{aligned} \tag{16}$$

(15) and (16) imply that

$$\begin{aligned}
\|z_{i-1}(n)\| + \|\delta x_{i-1}(n)\| &\le m_1\left(\|z_{i-1}(n-1)\| + \|\delta x_{i-1}(n-1)\|\right)\\
&\quad + m_2\|u_d(n-1) - u_{i-1}^f(n-1)\| + k_4
\end{aligned} \tag{17}$$

where m_1, m_2 are some suitably defined positive constants and $k_4 = q_0\varepsilon_3 + a_2\Delta T s_0\varepsilon_3 + a_1\varepsilon_2\Delta T$. Solving (17) will get

$$\begin{aligned}
&\|z_{i-1}(n)\| + \|\delta x_{i-1}(n)\|\\
&\le m_1^n\left(\|z_{i-1}(0)\| + \|\delta x_{i-1}(0)\|\right) + \sum_{j=0}^{n-1} m_1^{n-1-j} m_2\|u_d(j) - u_{i-1}^f(j)\|\\
&\quad + \sum_{j=0}^{n-1} m_1^{n-1-j} k_4\\
&\le \sum_{j=0}^{n-1} m_1^{n-1-j} m_2\|u_d(j) - u_{i-1}^f(j)\| + k_5
\end{aligned} \tag{18}$$

where k_5 is a suitably defined positive constant depending on and $z_{i-1}(0) = 0$. Substituting (18) into (14), we have

$$\begin{aligned}
&\|u_d(n) - u_i^f(n)\|\\
&\le \rho\|u_d(n) - u_{i-1}^f(n)\| + \sum_{j=0}^{n-1} g m_1^{n-1-j} m_2\|u_d(j) - u_{i-1}^f(j)\| + \varepsilon
\end{aligned} \tag{19}$$

for some positive constants ε. Let $\delta u_i^f(n) = u_d(n) - u_i^f(n)$, (19) can be rewritten as

$$\|\delta u_i^f(n)\| \le \rho\|\delta u_{i-1}^f(n)\| + \sum_{j=0}^{n-1} \beta\|\delta u_{i-1}^f(j)\| + \varepsilon \tag{20}$$

For some $\beta > 0$. The inequality (20) can be rearranged into the following matrix form of

$$\begin{bmatrix} \|\delta u_i^f(0)\| \\ \|\delta u_i^f(1)\| \\ \vdots \\ \|\delta u_i^f(N)\| \end{bmatrix} \le \begin{bmatrix} \rho & 0 & \cdots & 0 \\ \beta & \rho & \ddots & 0 \\ \vdots & \ddots & \ddots & \vdots \\ \beta & \cdots & \beta & \rho \end{bmatrix} \begin{bmatrix} \|\delta u_{i-1}^f(0)\| \\ \|\delta u_{i-1}^f(1)\| \\ \vdots \\ \|\delta u_{i-1}^f(N)\| \end{bmatrix} + \begin{bmatrix} \varepsilon \\ \varepsilon \\ \vdots \\ \varepsilon \end{bmatrix}$$

The above equation is now rewritten as a matrix form of $\delta U(i) \le A\delta U(i-1) + I_\varepsilon$ with the solution as follows,

$$\delta U(i) \le A^i \delta U(0) + \sum_{j=0}^{i-1} A^j I_\varepsilon \tag{21}$$

Since matrix A is a triangular matrix with all the eigenvalues less than 1, we conclude that

$$\lim_{i\to\infty} \delta U(i) \le \lim_{i\to\infty} A^i \delta U(0) + \lim_{i\to\infty} \sum_{j=0}^{i-1} A^j I_\varepsilon = \varepsilon \begin{bmatrix} \frac{1}{1-\rho} \\ \frac{\beta+1-\rho}{(1-\rho)^2} \\ \vdots \\ \frac{(\beta+1-\rho)^{N-1}}{(1-\rho)^N} \end{bmatrix}$$

This implies that there exists a constant $g_1 > 0$ such that

$$\lim_{i\to\infty} \max_n \left\| \delta u_i^f(n) \right\| = \lim_{i\to\infty} \max_n \left\| u_d(n) - u_i^f(n) \right\| \le \varepsilon g_1$$

By using (18), we have

$$\begin{aligned} \lim_{i\to\infty} \left\| \delta x_{i-1}(n) \right\| &\le \lim_{i\to\infty} (\left\| z_{i-1}(n) \right\| + \left\| \delta x_{i-1}(n) \right\|) \\ &\le \sum_{j=0}^{n-1} m_1^{n-1-j} m_2 \lim_{i\to\infty} \left\| u_d(j) - u_{i-1}^f(j) \right\| + k_5 \\ &\le \varepsilon g_2 + k_5 \end{aligned}$$

for some constant $g_2 > 0$. Thus we can conclude that

$$\begin{aligned} \lim_{i\to\infty} \left\| y_d(n) - y_i(n) \right\| &\le \lim_{i\to\infty} \left\| C x_d(n) - C x_i(n) - \xi_i(n) \right\| \\ &\le c\varepsilon h_2 + c k_5 + \varepsilon_3 \equiv \sigma \end{aligned}$$

IV. THREE TYPES OF DESIGN STRATEGY

Basically, the traditional feedforward sampled-data ILC is often applied as follows,

$$\begin{aligned} u_i(nh) &= (1-\alpha) u_{i-1}(nh) + \alpha u_0(nh) \\ &\quad + L_{i-1}(nh)(e_{i-1}((n+1)h) - e_{i-1}(nh)) \end{aligned} \tag{22}$$

where only the previous error is used in the design of ILC. However, it is well known that the learning performance is in general poor if the learning gain $L_{i-1}(nh)$ is not suitably chosen. Also as commented in our previous work [24], (22) will use more memory size when implementing the iterative learning controller in a digital circuit. In the following, we will discuss the design strategy from the consideration of both learning performance and memory capacity.

1. Type 1 Sampled-data ILC

The type I sampled-data ILC is designed using only the information of current error. The learning gain $L_{i-1}(nh)$ of feedforward iterative learning controller (5) is set to be zero and the feedback stabilization controller is designed as

$$u_i^b(nh) = K_P e_i(nh) + K_d(e_i(nh) - e_i((n-1)h)$$

In other words, the type I sampled-data iterative learning controller using current error design will become

$$\begin{aligned} u_i(nh) &= (1-\alpha) u_{i-1}(nh) + \alpha u_0(nh) \\ &\quad + K_P e_i(nh) + K_D(e_i(nh)) - e_i((n-1)h)) \end{aligned} \tag{23}$$

which is the one given in our previous work [24]. The main advantage of (23) is the reduction of memory size since only two sets of data, i.e., the previous input $u_{i-1}(nh)$ and the desired output $y_d(nh)$, are required for all $n \in \{0,1,2,\cdots,N\}$. Furthermore, the learning performance of (23) in the sense of learning rate is in general better than that of (22).

2. Type 2 Sampled-data ILC

Theoretically the learning performance will be better if both feedforward iterative learning controller and feedback stabilization controller are applied. Let the feedback stabilization controller is designed as a PD-type feedback controller similar to the type 1 sampled-data ILC, then the type 2 sampled-data ILC will take the form of

$$\begin{aligned} u_i(nh) &= (1-\alpha) u_{i-1}(nh) + \alpha u_0(nh) \\ &\quad + L_{i-1}(nh)(e_{i-1}((n+1)h) - e_{i-1}(nh)) \\ &\quad + K_P e_i(nh) + K_D(e_i(nh)) - e_i((n-1)h)) \end{aligned} \tag{24}$$

However, in addition to $u_{i-1}(nh)$ and $y_d(nh)$, we have to store the previous error $e_{i-1}(nh)$ so that we can get the one step ahead previous error $e_{i-1}((n+1)h)$ for the design of the type 2 sampled-data ILC.

3. Type 3 Sampled-data ILC

In the type 2 sampled-data ILC, the memory size increases mainly because that we have to use the one step ahead previous error $e_{i-1}((n+1)h)$ in the ILC design. Actually, the feedforward iterative learning controller can be treated as a D-type ILC in a digital formulation. The usage of $e_{i-1}((n+1)h) - e_{i-1}(nh)$ is to approximate the differential behavior in the continuous time domain, i.e., $\frac{d}{dt} e_{i-1}(t) \cong \frac{1}{h}(e_{i-1}((n+1)h) - e_{i-1}(nh))$. The term $e_{i-1}((n+1)h)$ is an important factor in (24) for theoretical analysis since it is utilized to guarantee the convergent condition (10). But the convergent condition (10) is ensured by two design parameters, one is the learning gain $L_{i-1}(nh)$ and the other is the forgetting factor α . It is noted that the learning condition (10) can be satisfied even if $L_{i-1}(nh) = 0$ as in the type 1 sampled-data ILC since $1-\alpha < 1$. This motivates us to modify the type 2 sampled-data ILC as follows,

$$\begin{aligned} u_i(nh) &= (1-\alpha) u_{i-1}(nh) + \alpha u_0(nh) \\ &\quad + L_{i-1}(nh)(e_{i-1}(nh) - e_{i-1}((n-1)h)) \\ &\quad + K_P e_i(nh) + K_D(e_i(nh)) - e_i((n-1)h)) \end{aligned} \tag{25}$$

In other words, we approximate the differential behavior by using $\frac{d}{dt} e_{i-1}(t) \cong \frac{1}{h}(e_{i-1}(nh) - e_{i-1}((n-1)h))$. Intuitively, the physical property of the approximation for differentiation in type 3 sampled-data ILC is almost equivalent to that in type 2 sampled-data ILC. This implies that the learning performance of type 3 sampled-data ILC will remain the same as that of type 2 sampled-data ILC and is in general better than that of type 1 sampled-data ILC. Using the data of $e_{i-1}(nh)$ and $e_{i-1}((n-1)h)$ instead of $e_{i-1}((n+1)h)$ enables us to reduce the memory capacity because it is not necessary to save the whole trajectories of previous input $u_{i-1}(nh)$ and previous error $e_{i-1}(nh)$ separately. For simplicity, let $u_0(nh)=0$ in (25). If we obtain $e_i(nh)$ and $e_i((n-1)h)$ at the sampling time instant n of ith iteration, we can compute the current input $u_i(nh)$ by using (25) supposing that the previous input $u_{i-1}(nh)$ and previous errors $e_{i-1}(nh)$, $e_{i-1}((n-1)h)$ are available in the memory. Once the values of $u_i(nh)$, $e_i(nh)$ and $e_i((n-1)h)$ are achieved, we can calculate $c_i(nh) \equiv (1-\alpha)u_i(nh)+L_i(nh)(e_i(nh)-e_i((n-1)h))$ and then store the data in the memory for the next iteration so that only one set of data is required. It is noted that the stored data is actually equivalent to the value of $(1-\alpha)u_{i-1}(nh)+L_{i-1}(nh)(e_{i-1}(nh)-e_{i-1}((n-1)h))$ in (25). This implies that only two sets of data, $y_d(nh)$ and $c_{i-1}(nh)$, are required in the memory for the use at the next iteration.

V. AN EXPERIMENT

In order to demonstrate the feasibility and effectiveness of the proposed three types of sampled-data iterative learning controller, we apply (23), (24) and (25) respectively to a DC motor system to execute a repetitive position tracking control experiments. The controller is implemented by a digital circuit written by using VHDL. The circuit code is compiled by ISE and then downloaded into a Xilinx FPGA chip. The hardware setup for the experiment is shown in Figure 1. It includes a DC servo motor, an FPGA control board and a PC. The experimental data is sent by the control code through an interface card to PC to store and show the output learning trajectory.

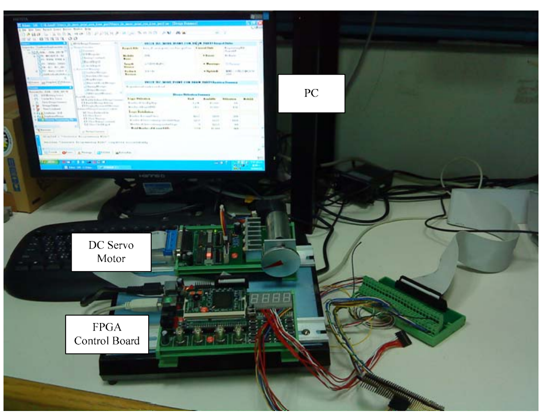


Figure 1: The hardware setup for experiment

In this experiment, the desired position trajectory is designed as in Figure 2. The desired position trajectory is designed to rotate clockwise the motor from the initial position to the final position of 90^o and then rotate the motor anticlockwise to the initial position for another 2 seconds. The sampling period h is 0.2 second so that there are 200 sampling data for one iteration.

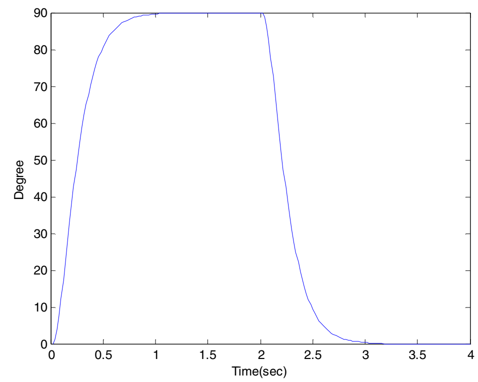
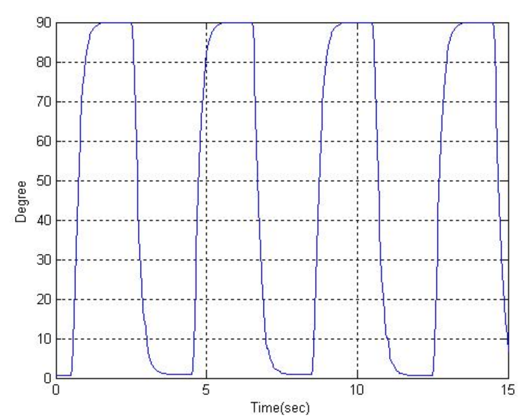


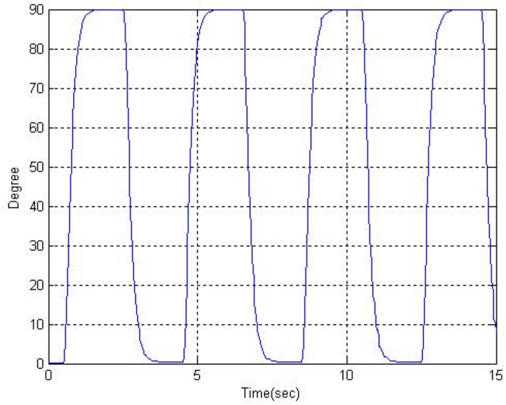
Figure 2: Desired position trajectory for one iteration

In these experiments, we set $\alpha = 0.09375$, $u_0(nh)=0$, $K_P=1$, $K_D=0.5$, $L_{i-1}(nh)=0.03125$ for the proposed sampled-data ILCs (23), (24) and (25). Figure 3 (a), (b), (c) show the learning performances after 4 trials respectively for the type 1 (23), type 2 (24) and type 3 (25) sampled-data ILCs. The rms values of the learning error after 4^{th} trial are 0.2734, 0.2213 and 0.2229 respectively for the type 1 (23), type 2 (24) and type 3 (25) sampled-data ILCs. Obviously, the pure feedback based type 1 sampled-data ILC has achieved nice learning control behavior for this practical application. But the learning performance can be even improved by using the type 2 or type 3 sampled-data ILC if the feedforward learning control mechanism is applied. We also would like to remark that the learning performance, including the learning speed and final learning error, are almost the same in many similar experiments for type 2 and type 3 sampled-data ILCs.

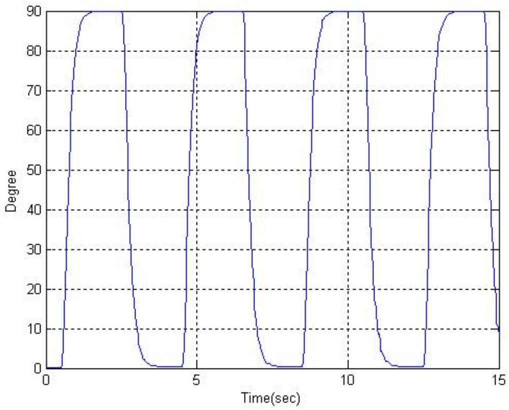
In this control experiment system, we use the Spartan3 XC3S1000 FPGA as the control chip. The percentages of number of occupied slices in this FPGA chip are 26%, 46% and 26% respectively for the type 1, type 2 and type 3 sampled-data ILCs. In summary, the above results show that the type 3 sampled- data ILC is a good choice for a repetitive learning control task from both performance improvement and memory capacity point of view.



(a)



(b)



(c)

Figure 3: The position trajectory of DC motor, (a) type 1 (b) type 2 (c) type 3 sampled-data ILC

VI. CONCLUSION

In this paper, we propose a sampled-data iterative learning controller based on feedforward and feedback structures and give a theoretical analysis as well as a real application. A technical proof is given to show the convergence of the learning system. The feedback controller is used to compensate for the output error to a small region such that the iterative learning controller can drive the error more quickly to a more reasonable value around zero. To further reduce the memory capacity due to the use of feedforward ILC, a new design concept is presented which not only remain the advantages of the feedforward and feedback design structure, but also keep the size of memory capacity as small as possible. In order to demonstrate the feasibility, the proposed three types of ILC algorithms are then implemented by a digital circuit. According to the experimental results, we prove that the theoretical design and the corresponding digital circuit are correct and feasible. Furthermore, the comparisons between the proposed three types sampled-data ILCs are discussed extensively from the point of performance improvement and memory capacity.

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